

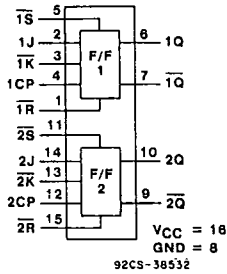
CD54/74HC109
CD54/74HCT109

T-46-07-07

High-Speed CMOS Logic

HARRIS SEMICONDUCTOR

27E D ■ 4302271 0017546 2 ■ HAS



FUNCTIONAL DIAGRAM

Dual J-K Flip-Flop with Set and Reset

Type Features:

- Positive-Edge triggered
- Asynchronous Set and Reset
- 60 MHz Typical Maximum Clock Frequency @ $V_{CC} = 5V, C_L = 15pF, T_A = 25^\circ C$
- Typical Propagation Delay = 18 ns @ $V_{CC} = 5V, C_L = 15pF, T_A = 25^\circ C$
- Schmitt Trigger Clock Inputs

The RCA-CD54/74HC109 and CD54/74HCT109 are dual J-K flip-flops with set and reset. The flip-flop changes state with the positive transition of Clock (1CP and 2CP).

The flip-flop is set and reset by active-low \bar{S} and \bar{R} , respectively. A low on both the set and reset inputs simultaneously will force both Q and \bar{Q} outputs high. However, both set and reset going high simultaneously results in an unpredictable output condition.

The CD54HC109 and CD54HCT109 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC109 and CD74HCT109 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (Over Temperature Range): Standard Outputs - 10 LSTTL Loads
- Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range: CD74HC/HCT: -40 to $+85^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Sigmetics
- CD54HC/CD74HC Types: 2 to 6 V Operation
- High Noise Immunity: $N_{IL} = 30\%, N_{IH} = 30\%$ of V_{CC} @ $V_{CC} = 5V$
- CD54HCT/CD74HCT Types: 4.5 to 5.5 V Operation
- Direct LSTTL Input Logic Compatibility $V_{IL} = 0.8V$ Max., $V_{IH} = 2V$ Min.
- CMOS Input Compatibility $I_i \leq 1 \mu A$ @ V_{OL}, V_{OH}

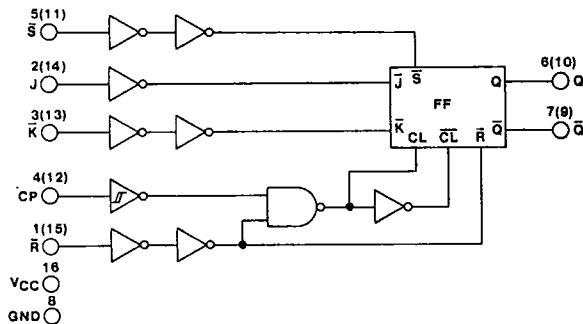


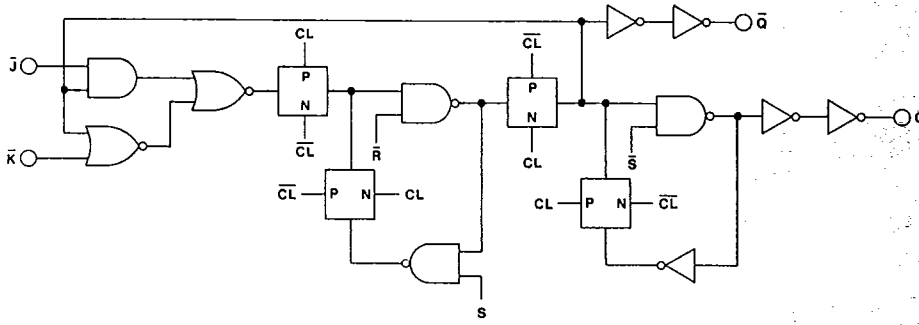
Fig. 1 - Logic diagram

TRUTH TABLE

Inputs					Outputs	
\bar{S}	\bar{R}	CP	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
L	L	X	X	X	L	H
L	L	X	X	X	H*	H*
L	H	X	L	X	L	H
H	H	X	L	L	L	H
H	H	X	L	H	H	L
H	H	X	L	H	H	L
H	H	X	L	X	H	L
H	H	X	H	L	L	H
H	H	X	H	H	H	L
H	H	X	H	X	H	L

*Unpredictable and unstable condition if both \bar{S} and \bar{R} go high simultaneously.

CD54/74HC109
CD54/74HCT109



DETAIL OF FLIP-FLOP

92CM-38536

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V _{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I _{IK} (FOR V _I < -0.5 V OR V _I > V _{CC} +0.5V)	± 20 mA
DC OUTPUT DIODE CURRENT, I _{OK} (FOR V _O < -0.5 OR V _O > V _{CC} +0.5 V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I _O) (FOR -0.5 V < V _O < V _{CC} +0.5 V)	± 25 mA
DC V _{CC} OR GROUND CURRENT (I _{CC}):	± 50 mA
POWER DISSIPATION PER PACKAGE (P ₀):	
For T _A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T _A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T _A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T _A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING -TEMPERATURE RANGE (T _A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T _{STG})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T _A = Full Package-Temperature Range) V _{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V _I , V _O	0	V _{CC}	V
Operating Temperature T _A :			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input rise and Fall Times t _r , t _f			
All inputs Except CP			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	
Input Rise and Fall Times t _r , t _f			
For CP			
at 2 V	0	unlimited	μs
at 4.5 V	0		
at 6 V	0		

*Unless otherwise specified, all voltages are referenced to Ground.

HARRIS SEMICONDUCTOR SECTOR 27E D 430227J 001754? 4 HAS

CD54/74HC109
CD54/74HCT109

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC109 / CD54HC109										CD74HCT109 / CD54HCT109										UNITS	
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES				
	V _I V	I _O mA	V _{CC} V	+ 25°C			-40/ + 85°C		-55/ + 125°C		V _I V	V _{CC} V	+ 25°C			-40/ + 85°C		-55/ + 125°C				
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max			
High-Level Input Voltage V _{IH}			2	1.5	—	—	1.5	—	1.5	—		4.5									V	
			4.5	3.15	—	—	3.15	—	3.15	—		to	2	—	—	2	—	2	—			
			6	4.2	—	—	4.2	—	4.2	—		5.5										
Low-Level Input Voltage V _{IL}			2	—	—	0.5	—	0.5	—	0.5		4.5									V	
			4.5	—	—	1.35	—	1.35	—	1.35		to	—	—	0.8	—	0.8	—	0.8	—		
			6	—	—	1.8	—	1.8	—	1.8		5.5										
High-Level Output Voltage V _{OH}	V _{IL} or V _{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{IL}	4.5	4.4	—	—	4.4	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—	or											
			6	5.9	—	—	5.9	—	5.9	—	V _{IH}											
TTL Loads	V _{IL} or V _{IH}	-4 -5.2	4.5	3.96	—	—	3.84	—	3.7	—	V _{IL}	4.5	3.98	—	—	3.84	—	3.7	—	V		
			6	5.48	—	—	5.34	—	5.2	—	or											
											V _{IH}											
Low-Level Output Voltage V _{OL}	V _{IL} or V _{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V _{IL}	4.5	—	—	0.1	—	0.1	—	0.1	—	V	
			4.5	—	—	0.1	—	0.1	—	0.1	or											
			6	—	—	0.1	—	0.1	—	0.1	V _{IH}											
TTL Loads	V _{IL} or V _{IH}	4 5.2	4.5	—	—	0.26	—	0.33	—	0.4	V _{IL}	4.5	—	—	0.26	—	0.33	—	0.4	—	V	
			6	—	—	0.26	—	0.33	—	0.4	or											
											V _{IH}											
Input Leakage Current I _I	V _{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	—	μA	
Quiescent Device Current I _{CC}	V _{CC} or Gnd	0	6	—	—	4	—	40	—	80	V _{CC} or Gnd	5.5	—	—	4	—	40	—	80	—	μA	
Additional quiescent Device Current ΔI _{CC} * per input pin: 1 unit load											V _{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	—	μA	

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
All	0.3

*Unit Load is I_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C

HARRIS SEMICONDUCTOR SECTOR 27E D 430227J 0017548 6 HAS

CD54/74HC109
CD54/74HCT109

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC	C_L (pF)	Typical		UNITS	
		54/74HC	54/74HCT		
Propagation Delay, CP → Q, \bar{Q}	t_{PLH} t_{PHL}	15	14	17	ns
$\bar{S} \rightarrow Q$	t_{PLH}	15	9	12	ns
$\bar{S} \rightarrow \bar{Q}$	t_{PHL}	15	13	19	ns
$\bar{R} \rightarrow Q$	t_{PHL}	15	15	19	ns
$\bar{R} \rightarrow \bar{Q}$	t_{PLH}	15	14	15	ns
CP Frequency	f_{MAX}	15	60	54	MHz
Power Dissipation Capacitance*	C_{PD} *	—	30	33	pF

* C_{PD} is used to determine the dynamic power consumption, per flip-flop.

$PD = C_{PD} V_{CC}^2 f_i + \sum V_{CC}^2 C_L f_o$ where:

f_i = Input Frequency

C_L = Output Load Capacitance

V_{CC} = Supply Voltage

f_o = Output Frequency

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITION	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Set-up Time J, \bar{K} to CP	t_{SU}	2	80	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	18	—	20	23	—	—	24	27	—	—	
		6	14	—	—	17	—	—	—	20	—	—	—	
Hold Time J, \bar{K} to CP	t_H	2	5	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	3	—	5	3	—	—	5	3	—	—	
		6	5	—	—	5	—	—	—	5	—	—	—	
Removal Time \bar{R} , \bar{S} to CP	t_{REM}	2	80	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	18	—	20	23	—	—	24	27	—	—	
		6	14	—	—	17	—	—	—	20	—	—	—	
Pulse Width CP, \bar{R} , \bar{S}	t_W	2	80	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	18	—	20	23	—	—	24	27	—	—	
		6	14	—	—	17	—	—	—	20	—	—	—	
CP Frequency	f_{MAX}	2	6	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	27	—	25	22	—	—	20	18	—	—	
		6	35	—	—	29	—	—	—	23	—	—	—	

HARRIS SEMICONDUCTOR SECTOR 27E D 4302271 0017549 8 HAS

CD54/74HC109
CD54/74HCT109

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	V _{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, CP → Q, \bar{Q}	t _{PHL}	2	175	—	—	220	—	—	—	265	—	—	ns	
	t _{PLH}	4.5	35	40	—	44	—	50	—	53	60	ns		
	t _{PHL}	6	30	—	—	37	—	—	—	45	—			
\bar{S} → Q	t _{PLH}	2	120	—	—	150	—	—	—	180	—	ns		
	t _{PLH}	4.5	24	30	—	30	38	—	36	45	ns			
	t _{PLH}	6	20	—	—	26	—	—	31	—				
\bar{S} → \bar{Q}	t _{PHL}	2	155	—	—	195	—	—	—	235	—	ns		
	t _{PHL}	4.5	31	45	—	39	56	—	47	68	ns			
	t _{PHL}	6	26	—	—	33	—	—	40	—				
R → Q	t _{PHL}	2	185	—	—	230	—	—	—	280	—	ns		
	t _{PHL}	4.5	37	45	—	46	56	—	56	68	ns			
	t _{PHL}	6	31	—	—	39	—	—	48	—				
\bar{R} → \bar{Q}	t _{PLH}	2	170	—	—	215	—	—	—	255	—	ns		
	t _{PLH}	4.5	34	37	—	43	46	—	51	56	ns			
	t _{PLH}	6	29	—	—	37	—	—	43	—				
Transition Times	t _{TLH}	2	75	—	—	95	—	—	—	110	—	ns		
	t _{THL}	4.5	15	15	—	19	19	—	22	22	ns			
	t _{THL}	6	13	—	—	16	—	—	19	—				
Input Capacitance	C _I	—	—	—	—	—	—	—	—	—	—	pF		

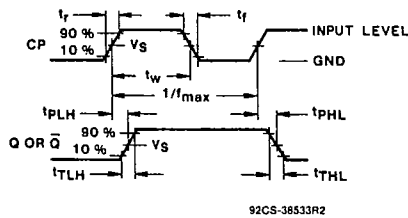


Fig. 2 - Clock to output delays and clock pulse width.

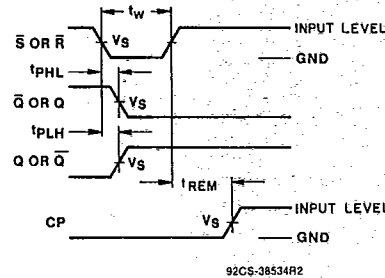


Fig. 3 - Reset or Set prerequisite and propagation delays.

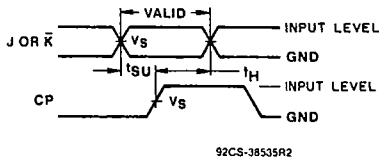


Fig. 4 - Data set-up and hold times.

	54/74 HC	54/74 HCT
Input Level	V _{CC}	3V
Switching Voltage, V _s	50% V _{CC}	1.3V

HARRIS SEMICONDUCTOR SECTOR 27E D 4302271 0017550 4 HAS